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10/775,592	02/09/2004	Byung Park	06847.P001	1757

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EXAMINER	
WYATT, KEVIN S	

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,592	PARK ET AL.	
	Examiner	Art Unit	
	Kevin Wyatt	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,8-22 and 30-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *38* is/are allowed.

6)☒ Claim(s) *1-5, 8-22 and 30-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the Request for Continued Examination and remarks filed on 10/23/2006. Currently, claims 1-5, 8-22 and 30-38 are pending.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4, 9-17, 20-22, and 30-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Merrill (Publication No. U.S. 2002/0036700 A1).

Regarding claim 1, Merrill shows in Fig. 8, a photodetecting array (320, i.e., 2 by 2 portion of array) comprising: a plurality of detecting cells (active pixel sensors, paragraph 0047, lines 1-2) laid out in an array on a substrate, comprising rows and columns of detecting cells; a plurality of gate lines, wherein each if the gate lines are coupled to a different row of more than two detecting cells (324-1 and 324-2, i.e., first and second row-select lines, paragraph 0049, lines 1-5); a plurality of data lines, wherein each of the data lines are (326-1 and 326-2, i.e.; column out lines) coupled to a different column of more than two detecting cells (paragraph 0050, lines 1-7); a plurality of main bias voltage lines (PIX-VCC lines), wherein each of the bias voltage lines are coupled to a different row of more than two detecting cells (324-1 and 324-2, i.e., row-select lines); and a plurality of additional bias voltage lines, wherein each of the additional bias voltage lines are coupled to two main bias voltage lines in different rows, wherein the gate lines and main bias voltage lines are laid out in a plurality of rows and the data lines and additional bias voltage lines are laid out in a plurality of columns

(paragraph 0046, lines 3-7, suggests that additional pixels could be added to each column or row depending on which size required. Therefore a third bias line could be added to accommodate additional pixels in either row without altering the structure of the array or departing from the concept of the invention).

Regarding claim 2, Merrill shows in Fig. 3, each of said plurality of detecting cells (110, i.e., active pixel cell sensor) comprises a transistor (116, 120,126, 130, 138, 144, or 148) and a photodiode (112), and wherein one of said plurality of gate lines is coupled to said transistor and one of said plurality of data lines is coupled to said diode (paragraph 0028 lines 17-19 and paragraph 0026, lines 6-8).

Regarding claim 4, Merrill shows in Figs. 3 and 8, that each photodiode (112) in said array is segmented from other photodiodes in said array (according to paragraph 0026 lines 3-4, there is only one photodiode per active pixel sensor).

Regarding claim 9, Merrill shows in Figs. 3 and 8, that said plurality of main bias voltage lines and plurality of additional bias voltage lines, together, form a staircase grid of bias voltage lines comprises a first plurality of main bias lines (PIX-VCC line to active pixel sensor pertaining to row-selects 322-1 and 322-3) which are laid out parallel to and proximate to corresponding gate lines (324-1 and 324-2, i.e., row-selects) and a second plurality of additional bias lines (PIX-VCC line to active pixel sensor pertaining to row-selects 322-2 and 322-4) which are laid out parallel to and proximate to only a portion of said plurality of data lines (portion of column out lines (326-1 and 326-2) leading directly from column out terminal of active pixel sensor) said second plurality of additional bias lines being coupled electrically between said first plurality of main bias

lines.

Regarding claim 10, Merrill shows in Fig. 3 a capacitive coupling (capacitor (136) within each pixel) between said second plurality of additional bias lines (132, i.e., bias potential line) and said plurality of data lines (152, i.e., column out line) is limited substantially to said portion (capacitive coupling takes place within active pixel sensor, paragraph 0029, lines 1-7 and paragraph 0031, lines 3-4).

Regarding claim 11, Merrill shows in Figs. 3 and 8, a photodetecting device comprising: a first row of more than two detecting cells (322-1 and 322-2, i.e., active pixel cells), each having a transistor (116, 120,126, 130, 138, 144, or 148) and a photodiode (112); a second row of more than two detecting cells, each having a transistor (116, 120,126, 130, 138, 144, or 148) and a photodiode (112), said second row being adjacent to and parallel with said first row; a first gate line (324-1, row-select) coupled to said first row; a second gate line (324-2, row-select) coupled to said second row; a first main bias voltage line (PIX-VCC line to active pixel sensor pertaining to row-selects 322-1 and 322-2) line out parallel with and proximate to said first gate line (324-1, row-select) and coupled to more than two detecting cells in said first row (322-1 and 322-2, i.e., active pixel cells); a second main bias voltage line (PIX-VCC line to active pixel sensor pertaining to row-selects 322-3 and 322-4) line out parallel with and proximate to said second gate line (324-1, row-select) and coupled to over two detecting cells in said second row (322-3 and 322-4, i.e., active pixel cells).

Regarding claim 12, Merrill shows in Fig. 3, said first and said second main bias voltage lines provide.a reverse bias voltage (132, i.e., bias potential line, paragraph

0028, lines 5-7) to photodiodes in said first row of detecting cells and in said second row of detecting cells.

Regarding claim 13, Merrill shows in Fig. 8, a third additional bias voltage line laid out parallel with and proximate to a first data line, said third additional bias voltage line being electrically coupled between said first bias voltage line and said second main bias voltage line (paragraph 0053, lines 3-4). Paragraph 0046, lines 3-7, suggests that additional pixels could be added to each column or row depending on which size required. Therefore a third bias line could be added to accommodate additional pixels in either row (which would more appropriately placed between first and second bias lines) without altering the structure of the array or departing from the concept of the invention.

Regarding claim 14, Merrill shows in Fig. 8, a second data line; and a fourth additional bias voltage line laid out parallel with and proximate to said second data line, said fourth additional bias voltage line being electrically coupled to said second main bias voltage line and to a fifth main bias voltage line (paragraph 0053, lines 3-4). Paragraph 0046, lines 3-7, suggests that additional pixels could be added to each column or row depending on which size required. Therefore a fourth bias line (coupled to first and fifth bias lines) could be added to accommodate additional pixels in either column or row without altering the structure of the array or departing from the concept of the invention.

Regarding claim 15, said first data (326-1, i.e., column out) line and said second data line (326-2, i.e., column out) are laid out substantially perpendicular to said first gate line (324-1, row-select) and to said second gate line (324-2, row-select) and

wherein said third additional bias voltage line is not coupled to said fifth main bias voltage line and wherein said fourth additional bias voltage line is not coupled to said first main bias voltage line (paragraph 0053, lines 3-4).

Regarding claim 16, Merrill shows in Fig. 8, that said first gate line (324-1, row-select) is coupled to transistors in said first row of detecting cells (322-1 and 322-2, i.e., active pixel cells) and said second gate line (324-2, row-select) is coupled to transistors in said second row of detecting cells (322-3 and 322-4, i.e., active pixel cells).

Regarding claim 17, Merrill shows in Fig. 3, that each photodiode in said first row and in said second row of detecting cells is segmented from other photodiodes.

Regarding claim 20, Merrill shows in Fig. 8 a photodetecting array (320, i.e., 2 by 2 portion of array) comprising: a plurality of detecting cells (active pixel sensors, paragraph 0047, lines 1-2) laid out in an array on a substrate, wherein said array comprises rows and columns of detecting cells, wherein each of the said detecting cells comprising a photodiode (112) and a transistor; a plurality of gate lines (324-1 and 324-2, i.e., first and second row-select lines, paragraph 0049, lines 1-5) laid out parallel to the rows of the array, wherein each of the gate lines are coupled to one of said rows of more than two detecting cells; a plurality of data lines (326-1 and 326-2, i.e., column out lines) laid out parallel to the columns of the array, wherein each of the data lines are coupled to one of said columns of detecting cells (paragraph 0050, lines 1-7); a mesh of bias voltage lines (PIX-VCC), said mesh comprising first main bias lines (PIX-VCC line to active pixel sensor pertaining to row-selects 322-2 and 322-4) disposed in a first direction which is laid out substantially parallel (324-1, i.e., row-select) to said gate lines

and second additional bias (PIX-VCC line to active pixel sensor pertaining to row-selects 322-1 and 322-3) lines disposed in a second direction which is laid out substantially perpendicular to said gate lines and wherein a total length of said first bias main lines exceeds a total length of said second additional bias lines (See Fig. 8).

Regarding claim 21, Merrill shows in Fig. 8 that said total length of said first main bias lines greatly exceeds said total length of said second additional bias lines by a factor of at least 10 times, and wherein said first main bias lines are proximate to corresponding said gate lines (first bias lines comprise a path substantially greater than the second bias lines, see Fig. 8).

Regarding claim 22, Merrill shows in Fig. 8 a method for manufacturing a photodetecting array, said method comprising: forming a plurality of gate lines; forming a plurality of transistor structures laid out in an array, the array comprising rows and columns; forming a plurality of data lines (326-1 and 326-2, i.e., column out lines) laid out in columns, wherein the data lines are coupled to said transistor structure over the transistors; forming a mesh of bias voltage lines (PIX-VCC), said mesh comprising first main bias (PIX-VCC line to active pixel sensor pertaining to row-selects 322-2 and 322-4) lines disposed in a first direction which is laid out substantially parallel to and proximate to said gate lines and second additional bias (PIX-VCC line to active pixel sensor pertaining to row-selects 322-1 and 322-3) lines disposed in a second direction which is laid out substantially perpendicular to said gate lines and wherein a total length of said first main bias lines exceeds a total length of said second additional bias lines (first bias lines comprise a path substantially greater than the second bias lines, see Fig.

8).

Regarding claim 30, Merrill shows in Fig. 8 the total length of the additional bias voltage lines are substantially less than the total length of the main bias voltage lines.

Regarding claim 31, Merrill shows in Fig. 3, the transistor is coupled to the gate line and the data line, and wherein the photodiode is coupled to the transistor and the bias voltage line (paragraph 0028, lines 17-19 and paragraph 0026, lines 6-8).

Regarding claim 31, Merrill shows in Fig. 3,the transistor is coupled to the gate line by a first pathway and to the data line by a second pathway, and wherein the photodiode is coupled to the transistor by a third pathway and to the main bias voltage line by a fourth pathway, wherein the first. second, third, and fourth pathways are all distinct and separate from each other (paragraph 0028, lines 17-19 and paragraph 0026, lines 6-8).

Regarding claim 32, Merrill shows in Fig. 8 the main bias voltage lines are laid out parallel to the gate lines and perpendicular to the data lines.

Regarding claim 33 and 35, Merrill shows in Fig. 3, the capacitive coupling between the plurality of bias voltage lines and the data lines are limited substantially to the proportional length of the additional bias voltage lines to the total length of the plurality of bias voltage lines (it is inherent that additional bias voltage lines in Merrill particularly of greater length would produce additional capacitive coupling); and wherein the additional bias voltage lines substantially reduces the resistance of the main bias voltage lines (additional bias voltage lines in Merrill would provide additional current paths thus reducing resistance).

Regarding claim 34, the capacitive coupling between the plurality of bias voltage lines and the data lines are limited substantially to the proportional length of the additional bias voltage lines to the total length of the plurality of bias voltage lines (it is inherent that additional bias voltage lines in Merrill particularly of greater length would produce additional capacitive coupling).

Regarding claim 36-37, Merrill shows in Fig. 3, that the transistor (126) is coupled to the gate line and the data line, and wherein the photodiode is coupled to the transistor (via, 126 and storage node (114)) and the main bias voltage line (132).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 5, 8, 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merrill (Publication No. U.S. 2002/0036700 A1) in view of Applicant's Admitted Prior Art (in Fig. 1).

Regarding claims 5 and 18, Merrill discloses the claimed invention as stated above. Merrill does not disclose that said photodiode in a cell is disposed above said transistor in said cell. Applicant's Admitted Prior Art shows in Fig. 1 that said photodiode (99) in a cell is disposed above said transistor (35) in said cell. It would have been obvious to one skilled in the art to apply the pixel structure of Applicant's Admitted Prior

Art to the device of Merrill for the purpose of providing maximum exposure to light to improve photodetection.

Regarding claims 3, 8 and 19, Merrill discloses the claimed invention as stated above. Merrill does not disclose that said photodiode comprises: an n+ layer formed over a first passivation layer; an amorphous silicon layer formed over said n+ layer; a p+ layer formed over said amorphous silicon layer; and a conductive layer formed over said p+ layer. Applicant's Admitted Prior Art shows in Fig. 1 that said photodiode comprises: an n+ layer (55) formed over a first passivation layer (40, i.e., SiON); an amorphous silicon layer (60, i.e., SiH) formed over said n+ layer (55); a p+ layer (65) formed over said amorphous silicon layer (60, i.e., SiH); and a conductive layer (70) formed over said p+ layer (65). It would have been obvious to one skilled in the art to apply the pixel structure of Applicant's Admitted Prior Art to the device of Merrill for the purpose of providing maximum exposure to light to improve photodetection.

Allowable Subject Matter

5. Claim 38 is allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 38, the prior art fails to disclose or make obvious a photodetecting array comprising, in addition to the other recited limitations of the claim, "a mesh of bias voltage lines, comprising additional bias lines and main bias lines, wherein each of the additional bias lines are coupled between at least a pair of main

bias lines; the mesh having a means for limiting capacitive coupling between the bias voltage lines and data lines."

Response to Arguments

6. Applicant's arguments filed 10/23/2006 have been fully considered but they are not persuasive.

In response to applicant's arguments that Merrill fails to disclose or suggest the features of amended claim 1, the examiner disagrees. The amended portions of claim 1 are not sufficient to overcome the anticipation of Merrill in particular, the recited limitation "main voltage lines" is still anticipated by Merrill.

In response to applicant's arguments that Merrill has failed to recognize the advantage of reducing the coupling capacitance between the main bias line and the data line, by forming a photodetecting array wherein the bias line and the data line are predominantly perpendicular to each other, instead of parallel. The examiner acknowledges that there appears to be no explicit disclosure in Merrill regarding the advantage of reducing the coupling capacitance between the main bias line and the data line. However, Merrill provides an embodiment such as illustrated in Fig. 8 which forms a photodetecting array wherein the bias line and the data line are predominantly perpendicular to each other.

In response to applicant's arguments that Merrill has failed to recognize the advantage of providing additional bias voltage lines that couples pairs of main bias lines, thus substantially reducing the resistance of the main bias lines, which reduces

the RC time constants associated with the main bias lines. The examiner acknowledges that Merrill does not disclose providing additional bias voltage lines that couples pairs of main bias lines. Therefore this subject matter has been cited as allowable subject matter.

In response to applicant's arguments that Merrill appears to disclose connection to components, but fails to disclose or suggest the actual physical location of the connections to the components, the examiner disagrees. The representation of the structure of Merrill is shown in Fig. 8, which illustrates location of the connections to each of the components.

In response to applicants arguments that AAPA fails to remedy the deficiencies of Merrill and in fact teaches away from the invention because AAPA discloses that the bias line and the data line are parallel, and therefore would have a high coupling capacitance, the examiner disagrees. The AAPA shown in Fig. 1 teaches the limitations of claims 3, 5, 8, and 18-19.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Wyatt whose telephone number is (571)-272-5974. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on (571)-272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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